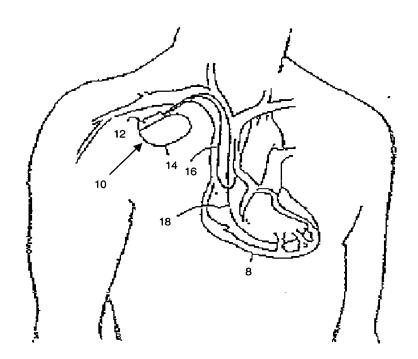
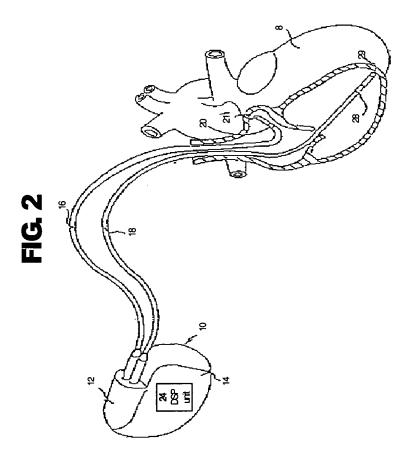
FIG. 1





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FIG. 4

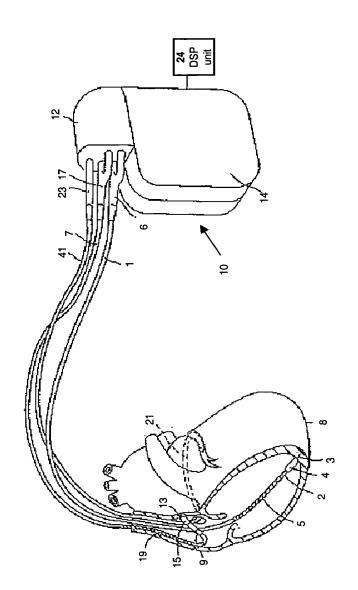


FIG. 5

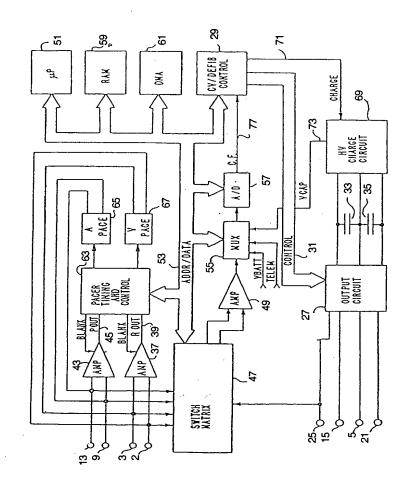


FIG. 6 600 610 605 615 Compression Compression 5 6 2 3 612 602 **620 FIRST INTERMEDIATE REGISTER** 2 3 5 6 7 ID 0 Once First Intermediate Register is Full 625 SECOND INTERMEDIATE REGISTER 9 10 11 12 13 14 15 2 3 8 5 635 FIRST OUTPUT REGISTER (full) 5 6 8 9 10 11 12 13 14 15 ID5 1 2 3 640 SECOND OUTPUT REGISTER (empty)

650 Storage

When Full

FIG. 7

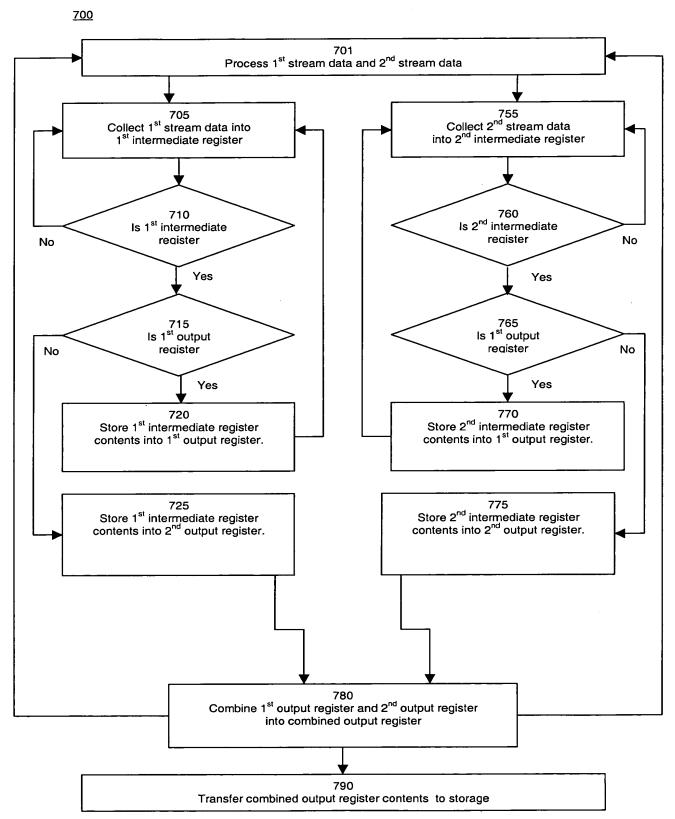
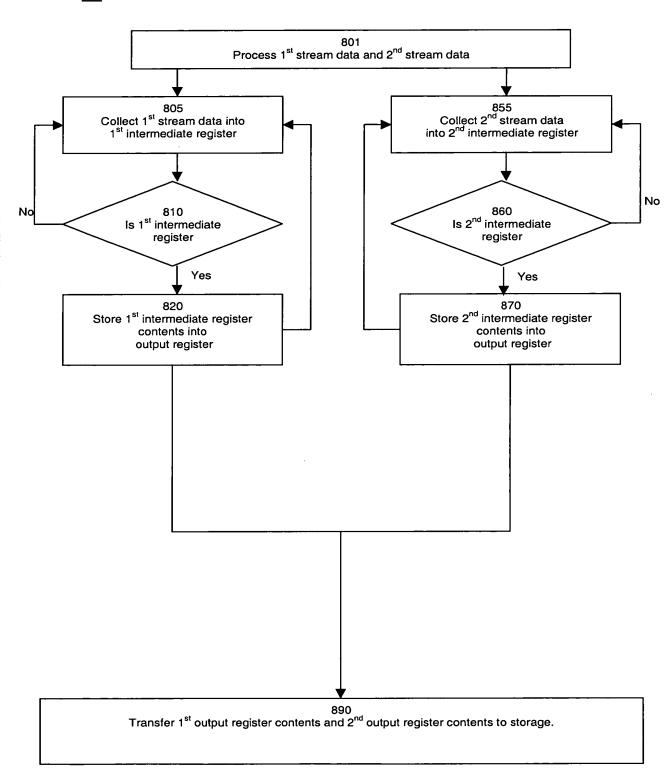




FIG. 8

<u>800</u>



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